REMARKS

Reassignment

This patent application has been assigned back to its inventors, Harry L. Tarnoff and Stuart T. Spence. A copy of the assignment was included with the letter of amendment dated April 6th, 2004, and was filed with the USPTO on that same date. The previous assignees, DFR2000, Inc., were owners of 100% of the rights, title and interest in the invention, and have assigned 100% of the rights, title and interest in the invention to the original inventors.

Pro Se

In view of the fact that the individual inventors of this invention are now 100% owners of the rights, title and interest in the invention, they wish to prosecute any amendments to the application Pro Se.

Discussion of Office Action and Rejection of Original Claims

The inventors recognize the basis for rejection by the examiner of claims 1-2, 4, 6, 8, 10, 12-13 and 16 under 35 U.S.C. 102(b) as being anticipated by Gunday et al. (US Patent No. 5,548,327), and of claim 7 being rejected under 35 U.S.C. 103(a) as being unpatentable over Gunday et al. (US Patent No. 5,548,327) in view of Sato (US Patent No. 5,838,363) and of claims 3,5,9,11 and 14-15 under 35 U.S.C. 103(a) as being unpatentable over Gunday et al. (US Patent No. 5,548,327). Specifically, the inventors agree with the examiner that the practice is well known to those experienced in the field to make a "trade-off" between cost and performance by designing circuits with different numbers of components, and to re-load the operating program to a Digital DSP or FPGA after power-on or to allow for upgrades.

General Discussion of Original Claims 1-16

The claims 1-16 of this application were written with the assistance of patent attorneys who are now no longer involved in any way with the application. After review of the basis for the examiner's rejection of claims 1-16, the inventors believe that the claims as filed did not properly represent the novel aspects of the invention. The invention under review more directly concerns the hardware structure of the interconnection of the components of the circuit, and we recognize that the claims 1-16 as filed do not make satisfactory reference to this structure.

Amendment of Independent Claims 1, 10, 14, and 16

Discussion of Circuit Interconnect Structure

This invention directly concerns the hardware structure of the interconnection of the components of the circuit. The design shows a formal grid structure having three or more groups of reprogrammable elements with selectable number of elements in each group whereby the interconnects on the circuit board allow for flexibility in modular design and reconfigurability on-the-fly. The prior art of Gunday et al. (US Patent No. 5,548,327) makes several references to the use of DSPs and FPGAs as providing system flexibility, but there is no mention in this patent of the use of a grid structure having three or more groups of reprogrammable elements with selectable number of elements in each group as a design criterion for the circuit interconnects as a way of improving the flexibility. The inventors have considerable experience in this field of circuit design, and do not know of any reference to a similar grid structure having three or more groups of reprogrammable elements with selectable number of elements in each group as a design criterion for the interconnects between components in a circuit. The inventors therefore respectfully submit that this novel design of a grid structure having three or more groups of reprogrammable elements with selectable number of elements in each group as a design criterion for the interconnects between components in a circuit is novel and useful, and is not obvious.

Detailed Discussion of the Circuit Interconnect Structure

The design in this application (Application No. 09/746,831) shows a formal grid structure having three or more groups of reprogrammable elements with selectable number of elements in each group whereby the interconnects on the circuit board allow for flexibility in modular design and reconfigurability on-the-fly. Figure 6 shows this unique structure where the FPGA elements are arranged in a two-dimensional form, and where some of the FPGA elements are used for inflow, other elements used for internal processing and still other elements for outflow. We refer the examiner particularly to paragraphs 15-18 and 98-103 and figures 4-6 of the application under consideration. Having this specific and highly advantageous hardware structure enables efficiency and parallel and multiple processing of digital images. This grid structure having three or more groups of reprogrammable elements with selectable number of elements in each group as a design criterion for the circuit interconnects allows multiple FPGAs to be employed in different situations where the data flow of the circuit paths can be optimized independently for each application. This Optimization would not be possible in conventional circuit designs where only the internal function of each individual FPGA can be reconfigured. Gunday et al clearly does not anticipate such a novel topology.

Specific advantages: (with references to paragraphs and figures in the application under consideration)

Specifically, it is highly advantageous:

(1) To have a single circuit board [para. 0098] that can be altered using software codes at any time to perform different film conversion functions and adapt to changes in format of digital motion picture files. [para. 0018]

(2) To have the physical structure of the film conversion device remain the same while the functions of the

film conversion device are redesigned to suit desired user needs. [para. 0098]

(3) To use "tiers" of elements to increase the throughput of desired functions [para. 0100]

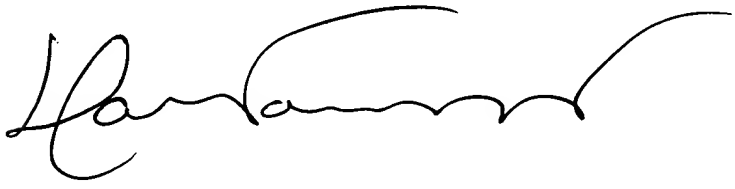
(4) To have a circuit layout which permits different FPGA populations (e.g. 6-6-9 as in para. 0102 or 3-0-6 or 12-12-12 as in para. 0103) where the choice of how to populate the circuit board is a production decision while the reconfigurability of these populations at any time is an end-user decision.

This grid structure having three or more groups of reprogrammable elements with selectable number of elements in each group as a design criterion for of the circuit layout gives the novel ability to the end-user to have a device which can optimally reconfigure itself automatically to include or exclude functions as the users' selections demand.

Request for Assistance from Examiner in Drafting Claims

As the inventors now with all rights to this invention acting Pro Se, we respectfully request assistance from the examiner pursuant to MPEP Section 707.07(j) to help us to develop a claim for the novel design of the apparatus we have described and a claim for the novel method of using this apparatus. We hope that in light of the above discussion, the examiner can assist with the development of claims in a way that better describes our invention and meets the U.S Patent requirements for novelty, usefulness and non-obviousness.

Very respectfully,



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